2137

Docket No. 4759-104 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of LEE et al.	:	Customer No. 26817
Serial No. 09/850,239	:	Group Art Unit: 2137
Filed: May 7, 2001	:	Examiner: CALLAHAN, Paul E.
Title: A METHOD AND SYSTEM FOR PERFORMING PERMUTATIONS WITH BIT PERMUTATION INSTRUCTIONS	:	Confirmation No. 2238

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

Sir:

In a December 20, 2004 Office Action, the Examiner required restriction to one of the following groups:

I. Claims 1-57 and 66-77, drawn to a method of performing an arbitrary permutation in a programmable processor via defining bit positions in a sequence of bits in a source register, to be permuted via a permutation instruction, and via assembly of the bits into a destination register, and repetition of the permutation operation on the bits assembled into the destination register, classified in class 380, subclass 265.

II. Claims 58-61, drawn to, a computer system for performing an arbitrary permutation comprising; a source register, a configuration register, a destination

register, and by use of a GRP, classified in class 712, subclass 8.

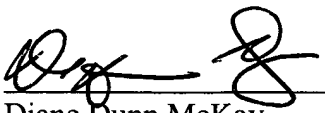
III. Claims 64 and 65, drawn to a circuit implementing a permutation instruction comprising a first matrix of a plurality of operation units each of which comprise a first input coupled to a first and a second input, and a control input where the control input controls the connection between the first and second inputs, a second matrix that is an inversion of the first, with the first matrix being selectively coupled to the second, classified in class 708, subclass 514.

Applicants hereby elect with traverse Group I, claims 1-57 and 66-77, drawn to a method of performing an arbitrary permutation in a programmable processor via defining bit positions in a sequence of bits in a source register, to be permuted via a permutation instruction, and via assembly of the bits into a destination register, and repetition of the permutation operation on the bits assembled into the destination register, classified in class 380, subclass 265 for prosecution in this application. Applicants submit that a search of the method of Group I would uncover a computer system of Group II and a circuit of Group III. Applicants respectfully request the right to file a divisional application directed to the unelected claims.

A prompt action on the merits is earnestly solicited. The Examiner is invited to telephone the undersigned should he believe this would expedite prosecution of this application. It is believed no fee is required. The Commissioner is authorized to charge any deficiency or credit any overpayment to Deposit Account No. 13-2165.

Respectfully submitted,

Dated: January 19, 2005



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